Claims

1. In a via-first dual damascene process involving the use of a low-K dielectric material as an insulation layer on a wafer substrate during the fabrication of an integrated circuit, a method for photolithographic patterning comprising the steps of:

filling an aperture etched into an insulation layer on a wafer substrate with a fill-in material for isolating the insulation layer from a photoresist layer deposited thereafter;

depositing a photoresist layer on the insulation layer;

exposing and developing the photoresist layer for providing a photoresist mask pattern for subsequent etching of the insulation layer; and

removing the fill-in material from the aperture.

2. The method as in claim 1, wherein the step of filling the aperture comprises the step of full filling the aperture.

3. The method as in claim 2, wherein the step of full filling the aperture comprises the step of full filling the aperture with antireflective coating.

4. The method as in claim 2, wherein the step of full filling the aperture comprises the step of full filling the aperture with a solvent based fill-in material.

5. The method as in claim 4, wherein the step of full filling the aperture with the solvent based fill-in material comprises the step of full filling the aperture with a water soluble fill-in material such as top antireflective coating.

6. The method as in claim 1, wherein the step of filling the aperture comprises the step of partially filling the aperture.

7. The method as in claim 6, wherein the step of partially filling the aperture comprises the step of lining the walls of the aperture.

8. The method as in claim 7, wherein the step of lining the walls of the aperture comprises the step of lining the walls of the aperture with conformal antireflective coating.

9. The method as in claim 8, wherein the step of lining the walls of the aperture with conformal antireflective coating comprises the step of lining the walls of the aperture with conformal antireflective coating to a thickness of 800 to 2000 angstroms.

10. The method as in claim 8, wherein the step of lining the walls of the aperture with conformal antireflective coating comprises the step of spinning onto the walls of the aperture the conformal antireflective coating.

11. In an integrated circuit manufactured using a via-first dual damascene process and having a low-K dielectric material as an insulation layer on a wafer substrate, a photolithographic pattern comprising:

an aperture etched into an insulation layer on a wafer substrate filled with a fill-in material for isolating the insulation layer from a photoresist layer deposited thereafter; and

a photoresist layer deposited on the insulation layer, in which the photoresist layer is exposed and developed for providing a photoresist mask pattern for subsequent etching of the insulation layer.

12. The pattern as in claim 11, wherein the aperture is fully filled.

13. The pattern as in claim 12, wherein the aperture is fully filled with antireflective coating.

14. The pattern as in claim 12, wherein the aperture is fully filled with a solvent based fill-in material.

15. The pattern as in claim 14, wherein the aperture is fully filled with a water soluble fill-in material such as top antireflective coating.

16. The pattern as in claim 11, wherein the aperture is partially filled.

17. The pattern as in claim 16, wherein the aperture is partially filled by lining the walls of the aperture.

18. The pattern as in claim 17, wherein the aperture is partially filled by lining the walls of the aperture with conformal antireflective coating.

19. The pattern as in claim 18, wherein the walls of the aperture is lined with conformal antireflective coating to a thickness of 800 to 2000 angstroms.

20. The pattern as in claim 18, wherein the conformal antireflective coating lining the walls of the aperture is spun onto the walls of the aperture.